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· Provides a hands-on guide to synthesis and timing analysis, using Synopsys Design Constraints (SDC), the industry-leading format for specifying constraints;

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This is article-3 of how to define Synthesis timing constraint Consider the example shown in Figure 1, where we have multiple clocks. As shown in Figure

2, the PLL is generating a main clock named CLKA of frequency 3 GHz, and there are 4 dividers generating CLKB, CLKC, CLKD and CLKE of frequency 333.3 MHz,...

Constraining Multiple Synchronous Clock Design in Synthesis

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This is article-5 of how to define Synthesis timing constraint Logically exclusive clocks are active in the design but cannot interact with each other. When dealing with logically exclusive clock, one often sees a mux with the select line determining which clock is active. An important guideline to

remember while dealing with logically exclusive clocks...